What Is Claimed Is:

1. A method of manufacturing a semiconductor wafer comprising:

forming a front-end structure over a semiconductor substrate;

forming a first layer of a back-end structure over said front-end structure, said first layer of a back-end structure having interconnects and regions of low-k material; and

etching a top surface of said first layer of a back-end structure, wherein a height of said regions of low-k material is less than a height of said interconnects.

2. The method of Claim 1 wherein said etching step comprises dry etch.

3. The method of Claim 2 wherein said etching step comprises plasma etch.

4. The method of Claim 3 wherein said plasma etch is a silicon carbide etch.

5. The method of Claim 1 wherein said etching step comprises wet etch.

6. The method of Claim 5 wherein said wet etch includes the use of a solvent.

7. The method of Claim 5 wherein said wet etch is deionized water.

8. The method of Claim 1 wherein said low-k material provides insulation for said interconnects.

9. The method of Claim 1 wherein said interconnects are metal lines that carry electrical signals and power.

10. The method of Claim 1 wherein said interconnects are vias that connect metal lines.

11. The method of Claim 1 wherein said regions of low-k material comprise OSG.

12. The method of Claim 1 wherein said interconnects comprise copper.

13. The method of Claim 1 wherein said height of said regions of low-k material is 10-30% less than said height of said interconnects.

14. The method of Claim 1 further comprising the step of forming a barrier layer over said first layer of a back-end structure.

15. The method of Claim 14 wherein said barrier layer comprises SiC.

16. The method of Claim 14 further comprising the step of forming a second layer of a back-end structure over said barrier layer, said second layer of a back-end structure having second layer interconnects and second layer regions of low-k material.

17. The method of Claim 16 further comprising the step of etching a top surface of said second layer of a back-end structure, wherein a height of said second layer regions of low-k material is less than a height of said second layer interconnects.

18. The method of Claim 17 wherein said height of said second layer regions of low-k material is 10-30% less than said height of said second layer interconnects.

19. The method of Claim 1 further comprising the step of forming a second layer of a back-end structure over said first layer of a back-end structure, said second layer of a back-end structure having second layer interconnects and second layer regions of low-k material.

20. The method of Claim 19 further comprising the step of etching a top surface of said second layer of a back-end structure, wherein a height of said second layer regions of low-k material is less than a height of said second layer interconnects.

21. The method of Claim 20 wherein said height of said second layer regions of low-k material is 10-30% less than said height of said second layer interconnects.

22. The method of Claim 20 wherein said etching step comprises plasma etch.

23. A method of manufacturing a semiconductor wafer comprising:

forming a front-end structure over a semiconductor substrate;

forming a first layer of low-k material over said front-end structure,

forming holes through said first layer of low-k material;

forming a metal layer over said first layer of low-k material, said metal layer also filling said holes;

reducing a height of said metal layer to form first layer metal interconnects and expose a top surface of said first layer of low-k material; and

etching a top surface of said semiconductor wafer to make a height of said first layer of low-k material less than a height of said first layer metal interconnects.

24. The method of Claim 23 wherein said reducing step comprises a Chemical Mechanical Polish.

25. The method of Claim 23 wherein said etching step comprises plasma etch.

26. The method of Claim 25 wherein said plasma etch is a silicon carbide etch.

27. The method of Claim 23 wherein said first layer of low-k material provides insulation for said first layer metal interconnects.

28. The method of Claim 23 wherein said first layer metal interconnects are metal lines that carry electrical signals and power.

29. The method of Claim 23 wherein said first layer metal interconnects are vias that connect metal lines.

30. The method of Claim 23 wherein said first layer of low-k material comprises OSG.

31. The method of Claim 23 wherein said first layer metal interconnects comprise copper.

32. The method of Claim 23 wherein said holes are formed using a dielectric etch process.

33. The method of Claim 23 wherein said height of said first layer of low-k material is 10-30% less than said height of said first layer metal interconnects.

34. The method of Claim 23 further comprising the step of forming a barrier layer over first layer of low-k material and first layer metal interconnects.

35. The method of Claim 34 wherein said barrier layer comprises SiC.

36. The method of Claim 34 further comprising the steps of:

forming a second layer of low-k material over said barrier layer,

forming holes through said second layer of low-k material;

forming a metal layer over said second layer of low-k material, said metal layer also filling said holes;

reducing a height of said metal layer to form second layer metal interconnects and expose a top surface of said second layer of low-k material; and

etching a top surface of said semiconductor wafer to make a height of said second layer of low-k material less than a height of said second layer metal interconnects.

37. The method of Claim 36 wherein said height of said second layer of low-k material is 10-30% less than said height of said second layer metal interconnects.

38. The method of Claim 23 further comprising the steps of:

forming a second layer of low-k material over said first layer of low-k material,

forming holes through said second layer of low-k material;

forming a metal layer over said second layer of low-k material, said metal layer also filling said holes;

reducing a height of said metal layer to form second layer metal interconnects and expose a top surface of said second layer of low-k material; and

etching a top surface of said semiconductor wafer to make a height of said second layer of low-k material less than a height of said second layer metal interconnects.

39. The method of Claim 38 wherein said height of said second layer of low-k material is 10-30% less than said height of said second layer metal interconnects.

40. The method of Claim 34 wherein said barrier layer is also an etch stop layer.

41. The method of Claim 34 wherein said barrier layer is also an adhesion layer.

42. The method of Claim 34 wherein said barrier layer is prevents diffusion of said first layer metal interconnects.

43. An integrated circuit comprising:

a semiconductor substrate;

a front-end structure coupled to said semiconductor substrate; and

a first layer of a back-end structure coupled to said front-end structure, said first layer of a back end structure having first layer interconnects and first layer dielectrics;

wherein a height of said first layer dielectrics is less than a height of said first layer interconnects.

44. The integrated circuit of Claim 43 wherein said first layer dielectrics comprises low-k material.

45. The integrated circuit of Claim 44 wherein said low-k material comprises OSG.

46. The integrated circuit of Claim 43 wherein said first layer interconnects comprises copper.

47. The integrated circuit of Claim 43 wherein said first layer interconnects are metal lines that carry electrical signals and power.

48. The integrated circuit of Claim 43 wherein said height of said first layer dielectrics are 10-30% less than said height of said first layer interconnects.

49. The integrated circuit of Claim 43 further comprising a barrier layer coupled to said first layer of a back-end structure.

50. The integrated circuit of Claim 49 wherein said barrier layer comprises SiC.

51. The integrated circuit of Claim 49 further comprising a second layer of a back-end structure coupled to said barrier layer, said second layer of a back-end structure having second layer interconnects and second layer dielectrics, wherein a height of said second layer dielectrics is less than a height of said second layer interconnects.

52. The integrated circuit of Claim 51 wherein said second layer dielectrics comprises low-k material.

53. The integrated circuit of Claim 52 wherein said low-k material comprises OSG.

54. The integrated circuit of Claim 51 wherein said second layer interconnects comprises copper.

55. The integrated circuit of Claim 51 wherein said second layer interconnects are metal lines that carry electrical signals and power.

56. The integrated circuit of Claim 51 wherein said height of said second layer dielectrics are 10-30% less than said height of said second layer interconnects.

57. The integrated circuit of Claim 51 wherein at least one of said first layer interconnects is electrically connected to at least one of said second layer interconnects at an interface region.

58. The integrated circuit of Claim 57 wherein said interface region is adjacent to an inside region of said barrier layer.

59. The integrated circuit of Claim 57 wherein said interface region is adjacent to an inside region of said second layer dielectric.

60. The integrated circuit of Claim 43 further comprising a second layer of a back-end structure coupled to said first layer of a back end structure, said second layer of a back-end structure having second layer interconnects and second layer dielectrics, wherein a height of said second layer dielectrics is less than a height of said second layer interconnects.

61. The integrated circuit of Claim 60 wherein said second layer dielectrics comprises low-k material.

62. The integrated circuit of Claim 61 wherein said low-k material comprises OSG.

63. The integrated circuit of Claim 60 wherein said second layer interconnects comprises copper.

64. The integrated circuit of Claim 60 wherein said second layer interconnects are metal lines that carry electrical signals and power.

65. The integrated circuit of Claim 60 wherein said height of said second layer dielectrics are 10-30% less than said height of said second layer interconnects.

66. The integrated circuit of Claim 60 wherein at least one of said first layer interconnects is electrically connected to at least one of said second layer interconnects at an interface region.

67. The integrated circuit of Claim 66 wherein said interface region is adjacent to an inside region of said second layer dielectric.

68. An integrated circuit comprising:

a semiconductor substrate;

a front-end structure coupled to said semiconductor substrate;

a first layer of a back-end structure coupled to said front-end structure, said first layer of a back end structure having first layer interconnects and first layer dielectrics, wherein a height of said first layer dielectrics is less than a height of said first layer interconnects;

a barrier layer coupled to said first layer of a back-end structure; and

a second layer of a back-end structure coupled to said barrier layer, said second layer of a back-end structure having second layer interconnects and second layer dielectrics, wherein a height of said second layer dielectrics is less than a height of said second layer interconnects;

further wherein at least one of said first layer interconnects is electrically connected to at least one of said second layer interconnects at an interface region.

69. The integrated circuit of Claim 68 wherein said interface region is adjacent to an inside region of said barrier layer.

70. The integrated circuit of Claim 68 wherein said interface region is adjacent to an inside region of said second layer dielectric.

71. The integrated circuit of Claim 68 wherein said height of said first layer dielectrics are 10-30% less than said height of said first layer interconnects.

72. The integrated circuit of Claim 68 wherein said height of said second layer dielectrics are 10-30% less than said height of said second layer interconnects.

73. An integrated circuit comprising:

a semiconductor substrate;

a front-end structure coupled to said semiconductor substrate;

a first layer of a back-end structure coupled to said front-end structure, said first layer of a back end structure having first layer interconnects and first layer dielectrics, wherein a height of said first layer dielectrics is less than a height of said first layer interconnects; and

a second layer of a back-end structure coupled to said first layer of a back-end structure, said second layer of a back-end structure having second layer interconnects and second layer dielectrics, wherein a height of said second layer dielectrics is less than a height of said second layer interconnects;

further wherein at least one of said first layer interconnects is electrically connected to at least one of said second layer interconnects at an interface region.

74. The integrated circuit of Claim 73 wherein said interface region is adjacent to an inside region of said second layer dielectric.

75. The integrated circuit of Claim 73 wherein said height of said first layer dielectrics are 10-30% less than said height of said first layer interconnects.

76. The integrated circuit of Claim 73 wherein said height of said second layer dielectrics are 10-30% less than said height of said second layer interconnects.